WHAT IS CLAIMED IS:

1. A circuit comprising:

an input stage including a first pair of input transistors wherein each of the transistors of the first pair of input transistors is coupled to a corresponding input terminal, and wherein the input terminals are operable to receive respective input signals;

a summing stage coupled to the input stage and including an output terminal, the summing stage configured to receive a plurality of signals from the input stage; and

a hysteresis feedback stage including an input terminal coupled to the output terminal of the summing stage, wherein the hysteresis feedback stage is further coupled to at least one summing node of the summing stage, and wherein the hysteresis feedback stage is operable to supply a current to the at least one summing node based on an output signal supplied at the output terminal of the summing stage.

2. The circuit of claim 1 wherein the hysteresis feedback stage comprises a first hysteresis transistor including a hysteresis transistor input terminal.

3. The circuit of claim 2 further comprising:

a second hysteresis transistor including a second hysteresis transistor input terminal coupled to the output terminal of the summing stage, wherein the second hysteresis transistor is further coupled to at least another summing node of the summing stage, and wherein the second hysteresis transistor is operable to supply a second current to the at least another summing node based on the output signal supplied at the output terminal of the summing stage; and

a first current limiting transistor coupled between a first current source and the first hysteresis transistor.

4. The circuit of claim 3 further comprising:

a bias circuit operable to provide a bias voltage to the first current limiting transistor and to a transistor controlling a current provided to the first pair of input transistors.

5. The circuit of claim 1 further comprising a control transistor operable to enable and/or disable the hysteresis feedback stage.

6. The circuit of claim 1 wherein the hysteresis feedback stage includes a current starved inverter.

7. The circuit of claim 1 wherein the input stage further comprises:

a second pair of input transistors wherein each of the transistors of the second pair of input transistors is coupled to a corresponding one of the input terminals.

8. The circuit of claim 7 wherein the first pair of input transistors is a differential pair of input transistors of a first type, and wherein the second pair of input transistors is a differential pair of input transistors of a second type.

9. The circuit of claim 1 wherein the summing stage includes a current mirror.

10. The circuit of claim 1 further comprising:

a programmable analog circuit block, the programmable analog circuit block having analog circuit block positive and negative input terminals and analog circuit block positive and negative output terminals;

an analog routing pool, the analog routing pool controlling the routing of at least one of: a signal provided by the programmable analog circuit block, a signal provided to the programmable analog circuit block, a signal provided to the input stage, and the output signal supplied at the output terminal of the summing stage.

11. The circuit of claim 10 further comprising:

a memory coupled to the analog routing pool, the memory storing information for use in programming the analog routing pool.

12. The circuit of claim 1 further comprising:

a digital to analog converter coupled to the input stage and operable to provide an analog signal to at least one of the first pair of input transistors.

13. A method of providing hysteresis in a comparator circuit, the method comprising:

controlling a first transistor with an output signal of a comparator circuit;

controlling a second transistor with the output signal of the comparator circuit;

limiting an amount of current available to at least one of the first transistor and the second transistor; and

applying an output current from at least one of the first transistor and the second transistor to a summing node of the comparator circuit.

14. The method of claim 13 wherein controlling the first transistor comprises:

routing the output signal of the comparator circuit to a gate terminal of the first transistor.

15. The method of claim 13 wherein limiting an amount of current available to at least one of the first transistor and the second transistor further comprises:

providing a current limiting transistor between a current sources and the at least one of the first transistor and the second transistor; and

biasing the current limiting transistor with a bias voltage from a bias circuit.

16. The method of claim 15 further comprising controlling a current available to an input stage of the comparator circuit using the bias voltage.

17. The method of claim 13 further comprising:

summing the output current from at least one of the first transistor and the second transistor with at least one output current from an input stage of the comparator circuit.

18. The method of claim 13 further comprising:

selectively enabling or disabling the at least one of the first transistor and the second transistor.

19. An apparatus comprising:

means for amplifying the difference between a first input signal and a second input signal;

means for summing a plurality of output signals from the amplifying means; and

means for providing a hysteresis signal to the summing means for amplifying the difference between a first input signal and a second input signal.

20. A comparator comprising;

an input amplifier including:

a first pair of input transistors having a first transistor type, each of the first pair of input transistors being coupled to a corresponding input terminal operable to receive a respective input signal;

a second pair of input transistors having a second transistor type, each of the second pair of input transistors being coupled to a respective one of the corresponding input terminals;

a first current mirror coupled to the first pair of input transistors and operable to sum a first pair of input amplifier output signals and

provide at least a portion of a comparator output signal on a comparator output terminal;

a second current mirror coupled to the second pair of input transistors and operable to sum a second pair of input amplifier output signals and provide at least another portion of the comparator output signal on the comparator output terminal;

a first hysteresis transistor including a first hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a first hysteresis current to at least one of the first current mirror and the second current mirror; and

a second hysteresis transistor including a second hysteresis transistor input terminal coupled to the comparator output terminal and operable to supply a second hysteresis current to at least one of the first current mirror and the second current mirror.